09/697305

ABSTRACT OF THE DISCLOSURE

The present invention provides a fault detecting method and a layout method for a semiconductor integrated circuit. The fault detecting method performs detection for faults in a semiconductor integrated circuit using a fault list corresponding to information on sites in the semiconductor integrated circuit where a fault is likely to occur or information required to reduce such faults. In addition, the fault detecting method and the layout method perform ordering of faults with their likelihood and weighting of the faults, taking into consideration physical information on a mask pattern within a chip or records of actual use of cells or functional blocks.